

## DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled ARRANGEMENT FOR INITIALIZING DIGITAL EQUALIZER SETTINGS BASED ON COMPARING DIGITAL EQUALIZER OUTPUTS TO PRESCRIBED EQUALIZED OUTPUTS

☒ is attached hereto      ☐ was filed on      as Application Serial No.      and was amended on      (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<b>Prior Foreign Application(s):</b>			<b>Priority Claimed</b>	
<u>Number</u>	<u>Country</u>	<u>Day/Month/Year filed</u>	<u>Yes</u>	<u>No</u>

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below.

<b>Prior Provisional Application(s):</b>	
<u>Application Number</u>	<u>Filing Date</u>

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

<b>Prior U. S. Application(s):</b>		
<u>Serial No.</u>	<u>Filing Date</u>	<u>Status: Patented, Pending, Abandoned</u>

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

and Richard J. Roddy, Reg. No. 27,688, Paul S. Drake, Reg. No. 33,491, Elizabeth A. Apperley, Reg. No. 36,428, Harry A. Wolin, Reg. No. 32,638, Bradley Botsch, Reg. No. 34,552, Michael Caywood, Reg. No. 37,797, Rajendra Jaipershad, Reg. No. 44,168, Daniel R. Collopy, Reg. No. 33,667 and Diana Robert, Reg. No. 36,654 with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to Customer No. 20736.

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Inventor's signature:

Date: 12-3-01

Citizenship: USA

Post Office Address: same as above

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Figure 1 consists of 12 sub-diagrams labeled (a) through (l), each showing a graph with 10 nodes arranged in a grid-like pattern. The nodes are labeled with numbers 1 through 10. The edges between nodes are represented by lines. In each diagram, certain edges are highlighted in red, indicating the current state of the algorithm. (a) shows the initial graph with all edges. (b) through (l) show the iterative process of adding and removing edges to form a minimum spanning tree. The red edges represent the edges that are currently in the tree or being considered for addition/removal. The diagrams illustrate the steps of the proposed algorithm, which involves finding a minimum spanning tree by iteratively adding and removing edges.